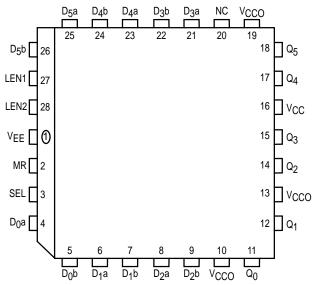
## 6-Bit 2:1 Mux-Latch

The MC10E/100E155 contains six 2:1 multiplexers followed by transparent latches with single-ended outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

- 850ps Max. LEN to Output
- 825ps Max. D to Output
- Single-Ended Outputs
- · Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E VEE Range of 4.2V to 5.46V
- 75kΩ Input Pulldown Resistors

### Pinout: 28-Lead PLCC (Top View)



\* All V<sub>CC</sub> and V<sub>CCO</sub> pins are tied together on the die.

### **PIN NAMES**

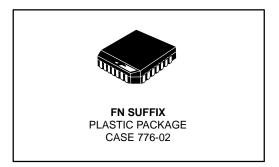
Pin	Function						
D <sub>0</sub> a – D <sub>04</sub>	Input Data a						
D <sub>0</sub> b – D <sub>4</sub> b	Input Data b						
SEL	Data Select Input						
LEN1, LEN2	Latch Enables						
MR	Master Reset						
$Q_0 - Q_4$	Outputs						

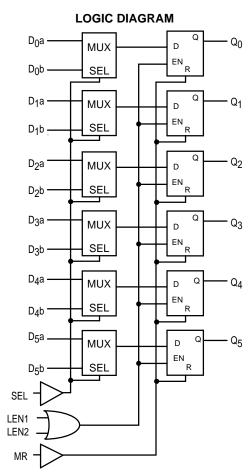
### **TRUTH TABLE**

SEL	Data
Н	a
L	b

# MC10E155 MC100E155

6-BIT 2:1 MUX-LATCH







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### **DC CHARACTERISTICS** (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
lіН	Input HIGH Current			150			150			150	μΑ	
IEE	Power Supply Current										mA	
	10E		85	102		85	102		85	102		
	100E		85	102		85	102		98	117		

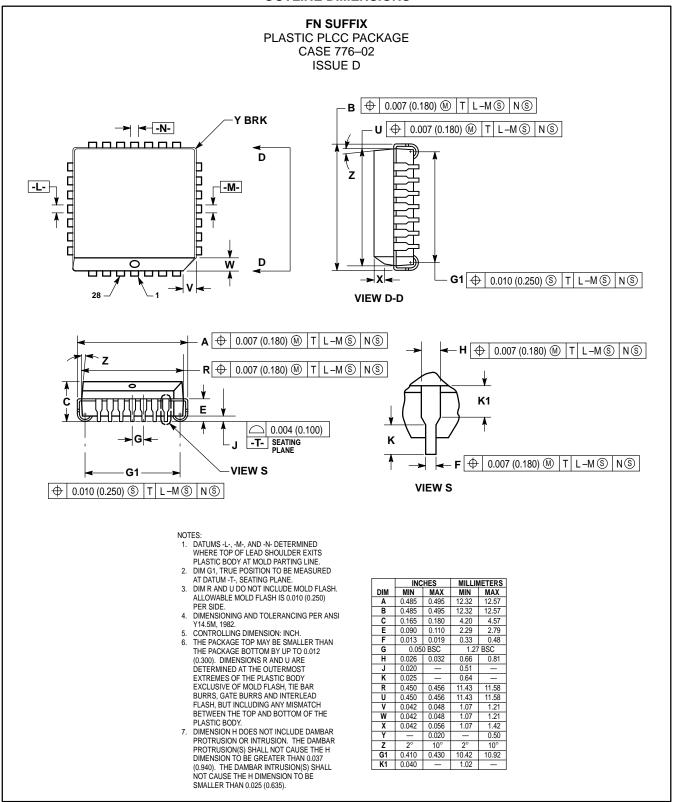
### **AC CHARACTERISTICS** ( $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$ ; $V_{CC} = V_{CCO} = GND$ )

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay to Output D SEL	325 475	500 675	700 925	325 475	500 675	700 925	325 475	500 675	700 925	ps	
	LEN MR	350 450	500 600	750 850	350 450	500 600	750 850	350 450	500 600	750 850		
t <sub>S</sub>	Setup Time D SEL	300 500	100 250		300 500	100 250		300 500	100 250		ps	
th	Hold Time D SEL	300 0	-100 - 250		300 0	-100 - 250		300 0	-100 - 250		ps	
tRR	Reset Recovery Time	800	650		800	650		800	650		ps	
tpW	Minimum Pulse Width MR	400			400			400			ps	
<sup>t</sup> SKEW	Within-Device Skew		75			75			75		ps	1
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Times 20 - 80%	300	450	800	300	450	800	300	450	800	ps	

<sup>1.</sup> Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA 2–2

#### **OUTLINE DIMENSIONS**



#### MC10E155 MC100E155

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